

OVERVIEW

The SiliconDrive EP 2.5" SATA Drive is an optimal time-to-market replacement for hard drives and flash cards or in host systems that require low power and scalable storage solutions.

SiliconDrive EP technology is engineered exclusively for the high performance, high reliability and multi-year product lifecycle requirements of the Enterprise System OEM market. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, video surveillance, storage networking, VoIP, wireless infrastructure, and interactive kiosks.

Every SiliconDrive EP is integrated with SiliconSystems patented PowerArmor and patent-pending SiSMART to virtually eliminate storage systems failures.

PowerArmor prevents data corruption and loss from power disturbances by integrating patented technology into every SiliconDrive EP.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

Numerous SiliconSystems patented and patent-pending application-specific technology can be integrated into SiliconDrive EP to safeguard application data and software IP. Application notes detailing these performance-enhancing options are available under NDA.

FEATURES

- RoHS 6 of 6 compliant
- Integrated PowerArmor and SiSMART technology
- Capacity range: 16GB to 64GB
- MTBF 2,000,000 hours
- SATA 3.0 Gbps compliant
- Hot-swappable



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REVISION HISTORY

Document No.	Release Date	Changes
4210DS-02DSR PRELIMINARY	September 30, 2008	Internal updates.
4210DS-01DSR PRELIMINARY	September 15, 2008	Internal updates.
4210DS-00DSR PRELIMINARY	August 14, 2008	Initial internal release.

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PHYSICAL SPECIFICATIONS

The SiliconDrive EP 2.5" SATA Drive are offered in an industry-standard 2.5" SATA Drive form factor. See ["Part Numbering" on page 56](#) for details regarding 2.5" SATA Drive capacities.

PHYSICAL DIMENSIONS

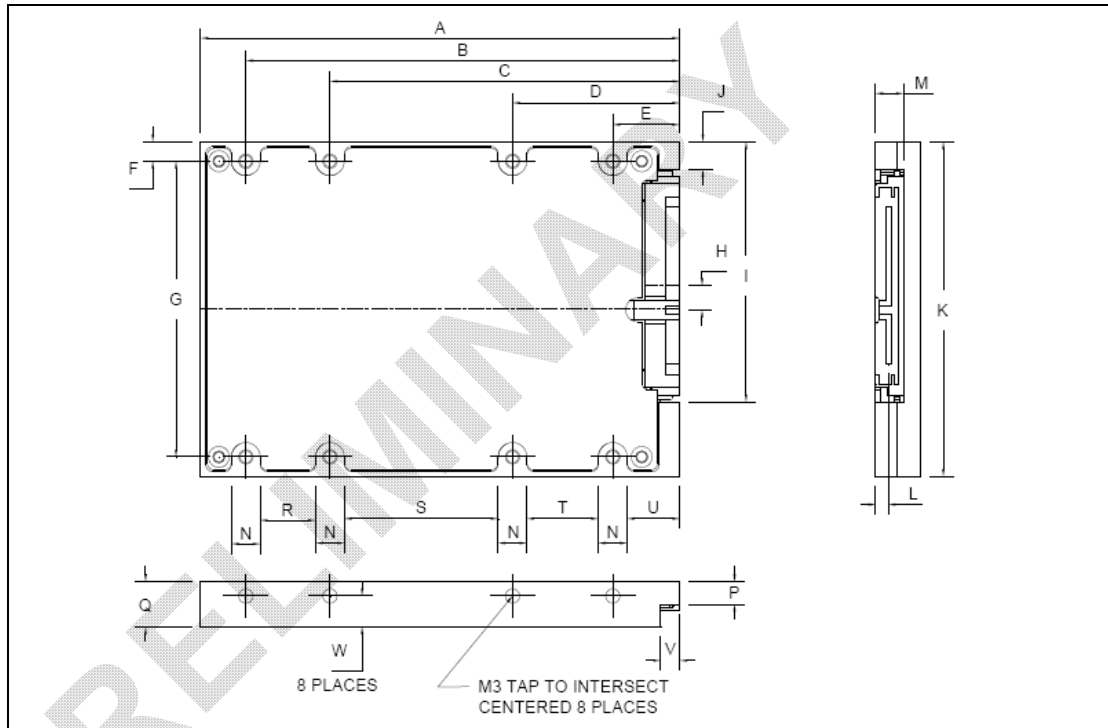


Figure 1: Physical Dimensions

Dimension	Millimeters	Dimension	Millimeters
A	100.00	L	2.65
B	90.60	M	5.82
C	73.03	N	6.00
D	34.93	P	4.75
E	14.00	Q	9.40
F	4.08	R	11.57
G	61.70	S	32.10
H	4.33	T	14.93
I	54.57	U	11.00
J	6.53	V	4.00
K	69.85	W	6.15

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PRODUCT SPECIFICATIONS

Note: All SiliconDrive EP 2.5" SATA Drive values quoted are typical at 25°C and nominal supply voltage.

SYSTEM PERFORMANCE

Table 1: System Performance

Read Transfer Rate (Typical)	50MBps
Write Transfer Rate (Typical)	50MBps
Burst Transfer Rate	3.0Gbps

SYSTEM POWER REQUIREMENTS

Table 2: System Power Requirements

DC Input Voltage	5.0 ± 10%
Sleep (Standby Current)	200mA
Read (Typical/Peak)	300mA
Write (Typical/Peak)	400mA

SYSTEM RELIABILITY

Table 3: System Reliability

MTBF (@ 25°C)	2,000,000 hours
Data Reliability	<1 non-recoverable error in 10 ³² bits read

PRODUCT CAPACITY SPECIFICATIONS

Table 4: Product Capacity Specifications

Product Capacity	Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/Track
16GB	16,391,208,960	32,014,080	16,383*	16	63
32GB	32,782,417,920	64,028,160	16,383*	16	63
64GB	65,564,835,840	128,056,320	16,383*	16	63

* = All IDE drives 8GB and larger use 16383 cylinders, 16 heads, and 63 sectors/track due to interface restrictions.

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ENVIRONMENTAL SPECIFICATIONS**Table 5: Environmental Specifications**

Temperature	0°C to 70°C (Commercial) -40°C to 85°C (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

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ELECTRICAL SPECIFICATION

PIN ASSIGNMENTS

The following tables describe the SiliconDrive EP 2.5" SATA Drive connector signals.

Table 6: SATA Signal Segment Pin Assignment

Pin #	Signal Name	Description
S1	Ground	Second mate.
S2	A+	Differential signal pair A.
S3	A-	Differential signal pair A.
S4	Ground	Second mate.
S5	B-	Differential signal pair B.
S6	B+	Differential signal pair B.
S7	Ground	Second mate.

Table 7: SATA Power Segment Pin Assignment

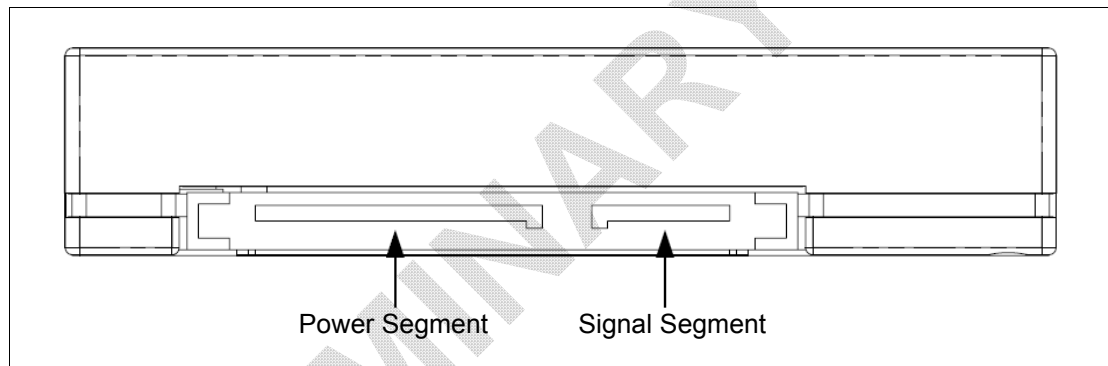
Pin #	Signal Name	Description
P1	V33	3.3V power (not used).
P2	V33	3.3V power (not used).
P3	V33	3.3V power (not used).
P4	GND	First mate.
P5	GND	Second mate.
P6	GND	Second mate.
P7	V5	5V power, pre-charge, second mate
P8	V5	5V power.
P9	V5	5V power.
P10	GND	Second mate.
P11	Reserved	Drive activity indicator/activity LED.
P12	GND	First mate.
P13	V12	12V pre-charge (not used).
P14	V12	12V power (not used).
P15	V12	12V power (not used).

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Notes:

- All pins are in a single row, with a 1.27mm (.050") pitch.
- The comments on the mating sequence in [Table 7](#) apply for backplane blind-mate connector cases only. In this situation, the mating sequences are:
 - Ground pins P4 and P12.
 - Precharge power pins and the other ground pins.
 - Signal pins and the rest of the power pins.
- There are three power pins for each voltage. One pin from each voltage is used for precharge in a backplane blind-mate situation.

**Figure 2: Serial ATA Pin Configuration****SILICONSYSTEMS PROPRIETARY**

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ABSOLUTE MAXIMUM RATINGS**Table 8: Absolute Maximum Ratings**

Symbol	Parameter	Minimum	Maximum	Units
T _S	Storage Temperature	-55	125	°C
T _A	Operating Temperature	-40	85	°C
V _{CC}	V _{CC} with Respect to GND	-0.3	6.7	V

DC CHARACTERISTICS**Table 9: DC Characteristics**

Symbol	Parameter	5V ± 10%		Units
		Minimum	Maximum	
V _{CC} 5V	Power Supply Voltage	4.5	5.5	V
I _{CCR}	I _{CC} Read Current	-	200	mA
I _{CCW}	I _{CC} Write Current	-	400	mA
I _{CCS}	I _{CC} Standby Current	-	300	mA

*(1) Except the pulled-up/pulled-down pin.

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ATA REGISTERS

DATA REGISTER

The Data register is a 16-bit register used to transfer data blocks between the host and drive buffers. The register may set to 8-bit mode by using the Set Features Command defined in "Seek — 7Xh" on page 38.

ERROR REGISTER

The Error register contains the error status, if any, generated from the last executed ATA command. The contents are qualified by the ERR bit being set in "Status Register" on page 14.

Table 10: Error Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	Bad Block Detected (BBK). Set when a bad block is detected.
6	Uncorrectable Data Error (UNC). Set when an uncorrectable error is encountered.
5	Media Changed (MC). Set to 0.
4	ID Not Found (IDNF). Set when the sector ID is not found.
3	MCR (Media Change Request). Set to 0.
2	Aborted Command (ABRT). Set when a command is aborted due to a drive error.
1	Track 0 Not Found (TKONF). Set when the execute drive diagnostic command is executed.
0	Address Mark Not Found (AMNF). Set in the case of a general error.

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FEATURE REGISTER

The Feature register is command-specific and used to enable and disable interface features. This register supports only either odd or even byte data transfers.

Table 11: Feature Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Feature Byte							

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SECTOR COUNT REGISTER

The Sector Count register is used to read or write the sector count of the data for which an ATA transfer has been made.

Table 12: Sector Count Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

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SECTOR NUMBER REGISTER

The Sector Number register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence, the device sets the register value to the last sector read or written as a result of the previous AT command.

When Logical Block Addressing (LBA) mode is implemented and the host issues a command, the contents of the register describe the Logical Block Number bits A[7:0]. Following an ATA command, the device loads the register with the LBA block number resulting from the last ATA command.

Table 13: Sector Number Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

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CYLINDER LOW REGISTER

The Cylinder Low register is set by the host to specify the cylinder number low byte. Following an ATA command, the content of the register is written by the device, identifying the cylinder number low byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Table 14: Cylinder Low Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

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CYLINDER HIGH REGISTER

The Cylinder High register is set by the host to specify the cylinder number high byte. Following an ATA command, the content of the register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Table 15: Cylinder High Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

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DRIVE/HEAD REGISTER

The Drive/Head register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3-0 of the head number in CHS mode or logical block number bits 27-24 in LBA mode.

Table 16: Drive/Head Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head register is used by the host to specify one of a pair of ATA drives present in the platform.

Bit(s)	Description
6	LBA. Selects between CHS (0) and LBA (1) addressing mode.
4	Drive Address (DRV). Indicates the drive number selected by the host, either 0 or 1.
3-0	<p>HS3 to 0. Indicates bits 3-0 of the head number in CHS addressing mode or LBA bits 27-24 in LBA mode.</p> <ul style="list-style-type: none"> • CHS to LBA conversion: $LBA = (C \times HpC + H) \times SpH + S - 1$ • LBA to CHS conversion: <ul style="list-style-type: none"> ◦ $C = LBA / (HpC \times SpH)$ ◦ $H = (LBA / SpH) \bmod (HpC)$ ◦ $S = (LBA \bmod (SpH)) + 1$ <p>...where:</p> <ul style="list-style-type: none"> ◦ C is the cylinder number ◦ H is the head number ◦ S is the sector count ◦ HpC is the head count per cylinder count ◦ SpH is the sector count per head count (track)

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STATUS REGISTER

The Status register provides the device's current status to the host. The status register is an 8-bit read-only register. When the contents of the register are read by the host, the IREQ# bit is cleared.

Table 17: Status Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	Busy (BSY). Set when the drive is busy and unable to process any new ATA commands.
6	Data Ready (DRDY). Set when the device is ready to accept ATA commands from the host.
5	Drive Write Fault (DWF). Always set to 0.
4	Drive Seek Complete (DSC). Set when the drive heads have been positioned over a specific track.
3	Data Request (DRQ). Set when a device is ready to transfer a word or byte of data to or from the host and the device.
2	Corrected Data (CORR). Always set to 0.
1	Index (IDX). Always set to 0.
0	Error (ERR). Set when an error occurs during the previous ATA command.

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COMMAND REGISTER

The Command register specifies the ATA command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Table 18: Command Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	ATA Command Code							

See ["ATA Command Block and Set Description" on page 19](#) for a listing of the supported ATA commands.

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ALTERNATE STATUS REGISTER

The Alternate Status register is a read-only register indicating the status of the device, following the previous ATA command. See ["Status Register" on page 14](#) for specific details.

Table 19: Alternate Status Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

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DEVICE CONTROL REGISTER

The Device Control register is used to control the interrupt request and issue ATA software resets.

Table 20: Device Control Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Write	-	-	-	-	1	SRST	nIEN	0

Bit(s)	Description
7-4	Reserved bits.
3	Always set to 1.
2	Software Reset (SRST) . When set, resets the ATA software.
1	Interrupt Enable (nIEN) . When set, device interrupts are disabled. There is no function in the memory-mapped mode.
0	Always set to 0.

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DEVICE ADDRESS REGISTER

The Device Address register is used to maintain compatibility with ATA disk drive interfaces.

Table 21: Device Address Register

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Bit(s)	Description
7	Reserved bit.
6	Write Gate (nWTG) . Low when a write to the device is in process.
5-2	nHS3 to nHS0 . The negated binary address of the currently selected head.
1	nDS1 . Low when drive 1 is selected and active.
0	nDS0 . Low when drive 0 is selected and active.

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ATA COMMAND BLOCK AND SET DESCRIPTION

In accordance with the *ANSI ATA Specification*, the device implements seven registers that are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol. A description of the ATA command block is provided in the following table.

Table 22: ATA Command Block and Set Description

Operation	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	1	LBA	1	Drive			X	
Command					X			

ATA COMMAND SET

Table 23: ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98h, E5h	-	-	-	-	D	-
1	Execute Drive Diagnostics	90h	-	-	-	-	D	-
1	Erase Sector	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	97h, E3h	-	Y	-	-	D	-
1	Idle Immediate	95h, E1h	-		-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA*	C8h	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y

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Table 23: ATA Command Set (Continued)

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Read Long Sector	22h, 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h, 21h	-	-	Y	Y	Y	Y
1	Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	Y	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	99h, E6h	-	-	-	-	D	-
1	Standby	96h, E2h	-	-	-	-	D	-
1	Standby Immediate	94h, E0h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
1	Write DMA*	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h, 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h, 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

* = This function does not apply to SiliconDrive EPs that have DMA disabled.

Notes:

- CY = Cylinder
- SC = Sector Count
- DH = Drive/Head
- SN = Sector Number
- FR = Feature LBA — LBA bit of the Drive/Head register (D denotes that only the drive bit is used)

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Check Power Mode — 98h, E5h

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode or is entering or exiting standby, the BSY bit is set, the Sector Count register set to 00h, and the BSY bit is cleared. In idle mode, BSY is set and the Sector Count register is set to FFh. The BSY bit is then cleared and an interrupt is issued.

Table 24: Check Power Mode — 98h, E5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive				
Command	98h or E5h							

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Executive Drive Diagnostic — 90h

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error register reports the appropriate diagnostic code.

Table 25: Executive Drive Diagnostic — 90h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X					Drive
Command								90h

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Format Track — 50h

The Format Track command formats the common solid-state memory array.

Table 26: Format Track — 50h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

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Identify Drive — ECh

Issued by the host, the Identify Drive command provides 256 bytes of drive attribute data (i.e., sector size, count, and so on) The identify drive data structure is detailed in the following table.

Table 27: Identify Drive — ECh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command					ECh			

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*Identify Drive — Drive Attribute Data***Table 28: Identify Drive — Drive Attribute Data**

Word Address	Data Default	Bytes	Data Description
0	045Ah	2	General configuration bit information <ul style="list-style-type: none"> • 15: Non-magnetic disk • 14: Formatting speed latency permissible gap needed • 13: Track Offset option supported • 12: Data Strobe Offset option supported • 11: Over 0.5% rotational speed difference • 10: Disk transfer rate > 10Mbps • 9: 10Mbps >= disk transfer rate > 5Mbps • 8: 5Mbps >= disk transfer rate • 7: Removable cartridge drive • 6: Fixed drive • 5: Spindle Motor Control option executed • 4: Over 15μs changing head time • 3: Non-MFM encoding • 2: Soft sector allocation • 1: Hard sector allocation • 0: Reserved
1	XXXXh	2	Number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of heads
4	0000h	2	Number of unformatted bytes per track
5	XXXXh	2	Number of unformatted bytes per sector
6	XXXXh	2	Number of sectors per track
7-8	XXXXh	4	Number of sectors per device
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number

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Table 28: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
20	0001h	2	Buffer type <ul style="list-style-type: none"> • 0000h: Not specified • 0001h: A single-ported, single-sector buffer • 0002h: A dual-ported multisector buffer • 0003h: A dual-ported multisector buffer with a read caching
21	0001h	2	Buffer size in 512-byte increments
22	0004h	2	Number of ECC bytes passed on read/write long commands
23-26	XXXXh	8	Firmware revision (eight ASCII characters)
27-46	XXXXh	40	Model number (40 ASCII characters)
47	8001h	2	15-8: Maximum number of sectors that can be transferred with a Read/Write Multiple command per interrupt
48	0000h	2	Double word (32 bit) not supported
49	0f00h	2	<ul style="list-style-type: none"> • 11: IORDY supported • 9: LBA supported • 8: DMA supported
50	0000h	2	Reserved
51	0200h	2	15-8: PIO data transfer cycle timing
52	0000h	2	15-8: DMA data transfer cycle timing
53	0007h	2	<ul style="list-style-type: none"> • 2: Word 88 is valid • 1: Words 64-70 are valid • 0: Words 54-58 are valid
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors
59	010Xh	2	7-0: Current sectors can be transferred with a Read/Write Multiple command per interrupt
60-61	XXXXh	4	Total number of sectors addressable in LBA mode

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Table 28: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
62	0000h	2	Single-word DMA modes supported
63	0007h	2	<ul style="list-style-type: none"> • 2: Multiword DMA mode 2 supported • 1: Multiword DMA mode 1 supported • 0: Multiword DMA mode 0 supported
64	0003h	2	7-0: Advanced PIO modes supported
65	0078h	2	15-0: Multiword DMA cycle time in nanoseconds
66	0078h	2	15-0: Multiword DMA transfer cycle time in nanoseconds
67	0078h	2	15-0: PIO mode cycle time without flow control
68	0078h	2	15-0: PIO mode cycle time with IORDY flow control
80	003Eh	2	<ul style="list-style-type: none"> • 5: ATA/ATAPI-5 supported • 4: ATA/ATAPI-4 supported • 3: ATA-3 supported • 2: ATA-2 supported • 1: ATA-2 supported • 0: Reserved
88	001Fh	2	<ul style="list-style-type: none"> • 4: UDMA mode 4 supported • 3: UDMA mode 3 supported • 2: UDMA mode 2 supported • 1: UDMA mode 1 supported • 0: UDMA mode 0 supported
163	0002h	2	2: Multiword DMA mode and PIO mode 6 supported

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Idle — 97h, E3h

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5ms, and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

Table 29: Idle — 97h, E3h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Timer Count (5ms increments)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	97h or E3h							

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Idle Immediate — 95h, E1h

When issued by the host, the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

Table 30: Idle Immediate — 95h, E1h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command					95h or E1h			

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Initialize Drive Parameters — 91h

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to 1 Fixed. Upon issuance of the command, the device sets the BSY bit and associated parameters, clears the BSY bit, and issues an interrupt.

Table 31: Initialize Drive Parameters — 91h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads — 1)			
Command	91h							

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Recalibrate — 1Xh

The Recalibrate command sets the cylinder low and high, head number to 0h, and sector number to 1h in CHS mode. In LBA mode (i.e., LBA = 1), the sector number is set to 0h.

Table 32: Recalibrate — 1Xh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	1	LBA	1	Drive			X	
Command								1Xh

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Read Buffer — E4h

The Read Buffer command allows the host to read the contents of the sector buffer. When issued, the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. When the data is ready, the DRQ bit is set and the BSY bit in the Status register are set and cleared, respectively.

Table 33: Read Buffer — E4h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command					E4h			

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Read DMA — C8h

The Read DMA command allows the host to read data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrive EPs that have DMA disabled.

Table 34: Read DMA — C8h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

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Read Multiple — C4h

The Read Multiple command executes similarly to the Read Sector command, with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

Table 35: Read Multiple — C4h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

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Read Sector — 20h, 21h

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count register. If the sector count is set to 0h, all 256 sectors of data are made available. When the command code is issued and the first sector of data has been transferred to the buffer, the DRQ bit is set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

Table 36: Read Sector — 20h, 21h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

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Read Long Sector(s) — 22h, 23h

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

Table 37: Read Long Sector(s) — 22h, 23h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

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Read Verify Sector(s) — 40h, 41h

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it does not set the DRQ bit and does not transfer data to the host. When the requested sectors are verified, the onboard controller clears the BSY bit and issues an interrupt.

Table 38: Read Verify Sector(s) — 40h, 41h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

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Seek — 7Xh

The Seek command seeks and picks up the head to the tracks specified in the task file. When the command is issued, the solid-state memory chips do not need to be formatted. After an appropriate amount of time, the DSC bit is set.

Table 39: Seek — 7Xh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

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Set Features — EFh

The Set Features command allows the host to configure the feature set of the device according to the attributes listed in [Table 41](#).

Table 40: Set Features — EFh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

Table 41: Set Features' Attributes

Feature	Operation
01h	Enable 8-bit data transfer
66h	Disable reverting to power on defaults
81h	Disable 8-bit data transfer
BBh	4 bytes of data apply on Read/Write Long commands
CCh	Enable revert to power on defaults

On power-up or following a hardware reset, the device is set to the default mode 81h.

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Set Multiple Mode — C6h

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

Table 42: Set Multiple Mode — C6h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count	Sector Count							
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command	C6h							

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Set Sleep Mode — 99h, E6h

The Set Sleep Mode command allows the host to set the device in sleep mode. When the onboard controller transitions to sleep mode, it clears the BSY bit and issues an interrupt. The device interface then becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

Table 43: Set Sleep Mode — 99h, E6h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command								99h or E6h

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Standby — 96h, E2h

When the Standby command is issued by the host, it transitions the device into standby mode. If the Sector Count register is set to a value other than 0h, the Auto Powerdown function is enabled and the device returns to Idle mode.

Table 44: Standby — 96h, E2h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count	Timer Count (5ms x Timer Count)							
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command	96h or E2h							

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Standby Immediate — 94h, E0h

When the Standby Immediate command is issued by the host, it transitions the device into standby mode.

Table 45: Standby Immediate — 94h, E0h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command	94h or E0h							

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Write Buffer — E8h

The Write Buffer command allows the host to rewrite the contents of the 512- byte data buffer with the wanted data.

Table 46: Write Buffer — E8h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive			X	
Command					E8h			

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Write DMA — CAh

The Write DMA command allows the host to write data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrive EPs that have DMA disabled.

Table 47: Write DMA — CAh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

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Write Multiple — C5h

The Write Multiple command operates in the same manner as the Write Sector command. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 48: Write Multiple — C5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

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Write Sector(s) — 30h, 31h

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 49: Write Sector(s) — 30h, 31h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

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Write Long Sector(s) — 32h, 33h

The Write Long Sector(s) command operates in the same manner as the Write Sector command — when issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 50: Write Long Sector(s) — 32h, 33h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

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Erase Sector(s) — C0h

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

Table 51: Erase Sector(s) — C0h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

PRELIMINARY

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Request Sense — 03h

The Request Sense command identifies the extended error codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error register.

Table 52: Request Sense — 03h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count					X			
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	1	X	1	Drive			X	
Command								03h

The extended error codes are defined in the following table.

Table 53: Extended Error Codes

Extended Error Codes	Description
00h	No error detected
01h	Self test is OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (requested head or sector invalid)
2Fh	Address overflow (address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30h-32h, 37h, 3Eh	Self test of diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed media format
03h	Write/erase failed

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Translate Sector — 87h

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive EP. If the host issues this command, the device responds with 0x00h in the data register.

Table 54: Translate Sector — 87h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

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Wear-Level — F5h

The Wear-Level command is supported as an NOP command for the purposes of backward compatibility with the ANSI AT attachment standard. This command sets the Sector Count register to 0x00h.

Table 55: Wear-Level — F5h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature					X			
Sector Count	Completion Status							
Sector Number					X			
Cylinder Low					X			
Cylinder High					X			
Drive Head	X	X	X	Drive				Flag
Command					F5h			

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Write Multiple w/o Erase — CDh

The Write Multiple w/o Erase command functions identically to the Write Multiple command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 56: Write Multiple w/o Erase — CDh

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

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Write Sector(s) w/o Erase — 38h

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 57: Write Sector(s) w/o Erase — 38h

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

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Write Verify — 3Ch

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command, with the added feature of verifying each sector written.

Table 58: Write Verify — 3Ch

Register	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

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SALES AND SUPPORT

To order or obtain information on pricing and delivery, contact your SiliconSystems Sales Representative.

PART NUMBERING

NOMENCLATURE

The following table defines the SiliconDrive EP 2.5" SATA Drive part numbering scheme.

Table 59: Part Numbering Nomenclature

SSD-	D	YYY	I	T	-4210 Part number suffix — contact your SiliconSystems' Sales Representative
					Temperature Range: • Blank = Commercial • I = Industrial
					Interface: S = SATA
					Capacity: 16G = 16GB to 64G = 64GB
					Form Factor: D = 2.5" Drive
SiliconSystems' SiliconDrive					

PART NUMBERS

The following table lists the SiliconDrive EP's part numbers.

Table 60: Part Numbers

Part Number	Capacity
SSD-D64GS(I)-4210	64GB
SSD-D32GS(I)-4210	32GB
SSD-D16GS(I)-4210	16GB

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ROHS 6 OF 6 PRODUCT LABELING — PB-FREE IDENTIFICATION LABEL



The Pb-free identification label indicates that the enclosed components/ devices and/or assemblies do not contain any lead (i.e., they are lead-free, as defined in RoHS directive 2002/95/ED). The above symbol is on all RoHS 6 of 6 compliant product labels, as seen in [Figure 3](#).

SAMPLE LABEL



Figure 3: Sample Label

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RELATED DOCUMENTATION

For more information, visit www.siliconsystems.com or contact your SiliconSystems Sales Representative.

Table 61: Related Documentation

SiliconDrive EP		
Application-Specific Description		Document Number
Technology		
PowerArmor	Eliminates drive corruption.	SSWPxx-PowerArmor-R
SiSMART	Calculates remaining useful life.	SSWPxx-SiSMART-R



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