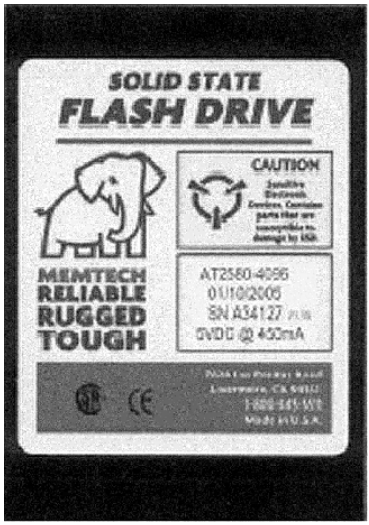
Panther Parallel ATA (PATA) Solid State Drive

Product Information Datasheet



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NOTE: This icon identifies information that relates to the safe operation of the equipment or related items.

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1 PRODUCT DESCRIPTION

1.1 OVERVIEW

Memtech's Panther Series Parallel ATA (PATA) Solid State Drives (SSDs) incorporate advanced Single-Level Cell (SLC) NAND flash memory technology to deliver state-of-the-art, non-volatile mass storage devices. Additional software device drivers are not required. Panther PATA SSDs are available in a 2.5-inch form factor, with a standard 44-pin IDE/ATA interface. Panther PATA SSDs are fully ATA-5 compliant and conform to the same mechanical and mounting requirements as standard rotating drives—making Panther SSDs easy-to-install, drop-in replacements for standard IDE/ATA-compliant hard disk drives (HDDs).

At the heart of the Panther PATA SSD is the Panther controller IC—providing the ATA interface to the host, and the IDE interface to the drive's local flash storage media. The Panther controller's integrated DMA controller interfaces with system memory to facilitate the seamless transfer of data between the host and the SSD.

Standard Panther SSDs are available with unformatted memory capacities ranging from 4 to 64 GB. Designed to operate in harsh environments, Panther PATA SSDs excel in ruggedness, reliability, compatibility and portability, and are ideal for applications that require high reliability and high tolerance to shock, vibration, humidity, altitude and temperature. And since there are no moving parts, Panther PATA SSDs are completely maintenance-free.

Panther PATA SSDs can operate at sustained data transfer rates of up to 40 MB per second. With power consumption kept to a minimum, Panther PATA SSDs can be powered from a single 5 volt source. The drive's solid state design eliminates electromechanical noise and delay inherent in traditional magnetic rotating media. Utilizing Memtech's patent-pending wear-leveling and bad-block mapping algorithms, Panther PATA SSDs ensure the consistency, accuracy, and integrity of user data. Superior data reliability is achieved through embedded error detection and correction code (EDC/ECC). The non-recoverable error rate of Panther PATA SSDs is less than 1 error per 10^{14} bits read.

Panther SSDs offer powerful user-customizable data sanitization (purge) features. Supporting both sanitized erase/fill and non-recoverable sanitization options, Panther SSDs can be configured to remove data from the drive, freeing storage space for later reuse, or to remove data and destroy the storage media—making the SSD unusable and data retrieval impossible. The drives's data security features comply with Department of Defense (DoD) and US military data security standards, including AFSSI 5020, AR 380-19, NAVSO P-5239-26, NISPOM DoD 5220.22-M and NSA 130-2.

1.1.1 Compatibility

Panther PATA SSDs can be installed in any machine running an operating system supporting ATA (IDE) bus specification standards.

1.1.2 Compliance and Conformity

The Panther PATA SSDs comply, in whole or in part, with the following standards:

Commercial	AS/NZS 3548 Class B, BSMI CNS 13438 Class B, CAN/CSA-V3/2001.04 (VCCI), CE (Conformite Europenne), CISPR 22 Class B, EN 55022 Class B, EN 61000-3-2, EN 61000-3-3, FCC Part 15 Class B, UL (Underwriter's Laboratory), NEBS Level 3, IEC 61000-4-2, IEC 61000-4-3, IEC 61000-4-4, IEC 61000-4-5, IEC 61000-4-6, IEC 61000-4-8, IEC 61000-4-11
Military	DoD 5220.22-M, MIL-STD-810F, NSA 130-2, AR 380-19, AFSSI 5020, Navso-P 5239, NEBS Level 3

1.2 STANDARD FEATURES

ATA/IDE Interface

- Conforms to ATA-5 Specification Standard

Performance

- Fast initialization
- Supports PIO modes 0 through 4
- Supports Ultra DMA modes 0 through 4
- Burst read/write performance up to 66 MB/sec
- Sustained read/write performance up to 40 MB/sec
- Field upgradeable firmware

Reliability

- Solid state design
- 10-year data retention
- Manual and automatic self-diagnostic tests
- Embedded EDC/ECC (Error Detection and Error Correction)
- SMART (Self-Monitoring, Analysis and Reporting Technology) endurance and reliability monitoring
- Dependable operation under unstable power conditions
- ATA bus connectors rated for over 10,000 insertions
- Rugged, impact-resistant aluminum casing
- 7 year warranty

Endurance

- Supports 2,000,000 write/erase cycles
- Supports unlimited read cycles
- Patent-pending wear-leveling algorithms
- Bad-block mapping algorithms

Physical

- 2GB to 64GB storage capacities available (unformatted)
- Industry standard 2.5-inch HDD form factor
- Compact design — only 9.5 mm thick (all models/capacities)

Environmental

- Meets or exceeds commercial and industrial temperature, humidity and altitude requirements
- Complies with MIL-STD 810F requirements for shock and vibration
  - 1500G, 0.5 ms half sine
  - 16.3G random, 5 - 2000 Hz

Compliance

- Meets NEBS Level 3 requirements for telco electrical environments
- Meets U.S. Army, Navy, Air Force and DoD security erase and sanitization (purge) guidelines

1.3 OPTIONAL FEATURES

- SMART status monitoring (see “SMART (Self-Monitoring, Analysis and Reporting Technology)” on page 20)
- Sanitization (see “Sanitize Erase/Fill” on page 22)

1.4 PHYSICAL CHARACTERISTICS

1.4.1 Drive Assembly Exterior Dimensions

Panther PATA SSD's internal components are housed in precision machined aluminum alloy enclosures. The outside dimensions of the drive are illustrated in Figure 1.

Thickness 0.0374 in (9.5 mm)

Width 2.75 in (69.8 mm)

Length (maximum) 3.94 in (100.2 mm)

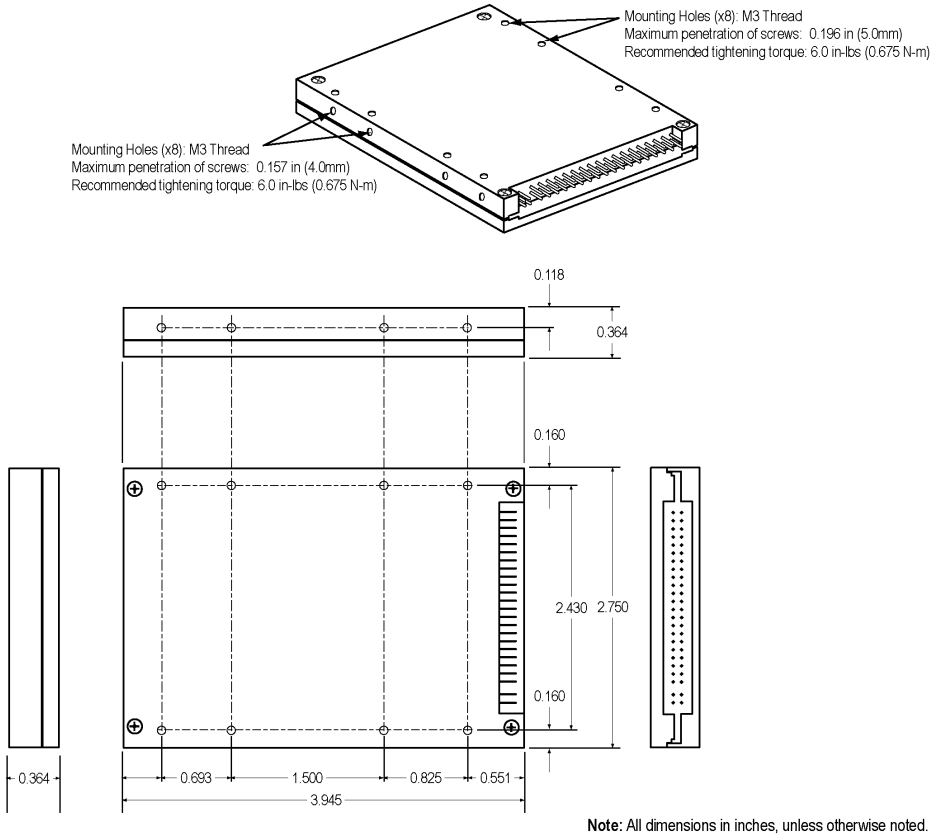

Figure 1. *2.5-inch Panther PATA SSD Assembly Drawing*

1.4.2 Drive Assembly Weight

The weight of a Panther PATA SSD varies, depending on the specific set of design characteristics of the drive. For example, a standard 32 GB, 2.5-inch Panther PATA SSD weighs approximately 0.322 lb (0.120Kg).

The following characteristics must be taken into consideration in order to determine the exact weight of a drive:

- Storage capacity
- IC stacking technology (if used)
- Flash controller/memory configuration
- Form factor

1.5 ENVIRONMENTAL CHARACTERISTICS

To validate the SSD's reliability and suitability for operation in harsh mobile environments, Panther PATA SSDs are subjected to a series of environmental tests.

1.5.1 Temperature, Humidity and Altitude

Panther PATA SSDs (all models) operate without degradation within the ambient temperature, relative humidity and altitude ranges specified in Table 1.

Table 1. *Environmental Conditions*

Operating Temperature	
Commercial:	0° to 70° C (32° to 158° F)
Industrial:	-40° to 85° C (-40° to 185° F)
Storage:	-55° to 95° C (-67° to 203° F)
Operating Humidity	5 - 95% relative, non-condensing
Altitude	125,000 ft.

1.5.2 Shock and Vibration

In setting the initial baseline for shock and vibration test levels, the Panther PATA SSD was exposed to increasingly harsh levels of stress until the drive's failure levels were determined. The tests were then repeated using the stress levels thereby established, to verify that the SSD would meet these specifications consistently. This process established the shock and vibration levels that have been used in subsequent shock and vibration testing.

1.5.2.1 Mechanical Shock

Panther PATA SSDs are shock-tested in accordance with MIL-STD-810F and operate as specified, without degradation, when subjected to the following:

Test Condition: Three 50G shocks (peak value, 11 ms duration, half-sine waveform) along the x, y and z axes.

Test Result: 1,500G operating shock

1.5.2.2 Random Vibration

Memtech Panther PATA SSDs are vibration-tested in accordance with MIL-STD-810F and operate as specified, without degradation, when subjected to the following:

Test Condition: Random vibration, between 20Hz and 2,000Hz along the x, y and z axes.

Test Result: 16.3G operating vibration

1.6 ELECTRICAL CHARACTERISTICS

1.6.1 Operating Voltage

Panther PATA SSDs require an input voltage of +5.0 Vdc ± 5% (4.75 - 5.25 Vdc).

1.6.2 Power Consumption

The amount of power consumed by Panther PATA SSDs is determined by the storage (memory) capacity of the drive, and the flash controller/memory configuration of the drive. Table 2 lists (by capacity) the power consumption of Panther PATA SSDs during typical operations at 5 Vdc.

Table 2. *Panther PATA SSD Typical Power Consumption (watts/mA)*

	8 GB	16 GB	24 GB	32 G	64 GB
Sustained Read/Write	2.50 watts/ 431 mA	2.15 watts/ 431 mA	2.15 watts/ 431 mA	2.15 watts/ 502 mA	2.15 watts/ 502 mA
Sanitized Erase/Fill (running low power option)	3.00 watts/ 600 mA	2.92 watts/ 583 mA	3.38 watts/ 675 mA	3.71 watts/ 741 mA	3.71 watts/ 741 mA
Data Transfer Rate	10-40 MB/sec	10-40 MB/sec	10-40 MB/sec	10-40 MB/sec	10-40 MB/sec

1.7 OPERATION AND PERFORMANCE CHARACTERISTICS

1.7.1 ATA (IDE) Bus Modes

Panther PATA SSDs support the following ATA operating modes:

- PIO Modes 0 through 4
- Ultra DMA Modes 0 through 4

1.7.2 Mount Time

The amount of time required to initialize and mount a Panther PATA SSD varies, depending on the operating system (Windows®, Linux®, etc.) in which the SSD is running and the storage capacity of the drive.

1.7.3 Seek Time

Unlike a magnetic rotating disk, the Panther PATA SSD has no moving head or platter. There is no seek time or rotational latency issues to contend with. Panther PATA SSDs dramatically improve transaction throughput, particularly for applications that are configured to take advantage of the characteristics of the drive.

1.7.4 Data Transfer Rate

The data transfer rate of Panther SSDs depends on the flash controller/flash memory configuration of the drive. The drive's scalable architecture is capable of accommodating sustained and burst data transfer rates as follows:

Sustained Read/Write Rates: 20, 30, and 40 MB/sec
Burst Read/Write Rate: 66 MB/sec

1.7.5 Endurance

The useful life of a flash media is limited by the number of write/erase operations that can be performed on the media. Typically, the write/erase cycles for flash media ranges between 100,000 and 300,000. To extend the useful life of Panther PATA SSDs, special wear-leveling and bad-block mapping algorithms are integrated in the drive's firmware—increasing the drive's overall endurance rating to 2,000,000 write/erase cycles.

1.7.5.1 Wear-Leveling

The dynamic wear-leveling algorithm integrated in the Panther PATA SSD's firmware guarantees that erase/write cycles are evenly distributed across all of the drive's flash memory block locations. Wear-leveling eliminates repeated writes to the same physical flash memory location, thereby preventing blocks from wearing out prematurely.

1.7.5.2 Bad-block Management

The Panther PATA SSD's bad-block mapping algorithm, replaces bad blocks with new ones from available spares. One percent (1%) of the Panther PATA SSD's flash memory is held in reserve (spare block) for bad block replacement. Bad blocks in the media are flagged when detected. The next time an attempt is made to access a flagged block, it is immediately replaced by a spare block. The drive's bad block mapping function enables data to be automatically transferred from a bad sector to an available spare block.

1.7.5.3 Data Retention

Data stored on Panther PATA SSDs remains valid for 10 years without requiring batteries or refreshing.

1.7.6 Reliability

1.7.6.1 Mean Time Between Failure (MTBF)

The average time Panther PATA SSDs work without failure is typically greater than 2,300,000 hours.

1.7.6.2 Error Detection and Correction

The SSD's error detection code and error correcting code (EDC/ECC) helps maintain data integrity by allowing single or multiple bit corrections to the data stored in the drive's flash array. If the data in the flash array is corrupted due to aging or during the programming process, EDC/ECC will compensate for the errors to ensure the delivery of accurate data to the host computer. The EDC/ECC engine on the Panther PATA SSD is capable of correcting up to two bytes in error and detecting up to 3 bytes in error. An extensive retry algorithm is also implemented on all Panther PATA SSDs, so that single event disturbances such as ESD or EMF occurring during a read operation can be readily overcome.

1.7.6.3 Built-in Self Test

During power-up, the SSD's micro controller tests Panther controller memory, and then performs a back-end status check to verify proper flash memory controller operations. If a fault condition is detected in the flash memory controller, the SSD's status is reported as failed.

2 FUNCTIONAL DESCRIPTION

2.1 PANTHER PATA SSD FUNCTIONAL BLOCKS

Memtech™ Panther series solid state drives comprise the following primary functional component blocks:

- ATA (IDE) Bus Interface
- SSD Control
- Flash Memory

2.1.1 ATA (IDE) Bus Interface Block

This section provides information on the ATA (IDE) Bus interface connectors used with 2.5-inch Panther PATA SSDs.

2.1.1.1 44-pin ATA Bus Connector

The 2.5-inch Panther-series SSDs are equipped with a 44-pin ATA bus connector (Figure 2, below), located on the rear of the drive. DC power and IDE bus traffic is supplied through a non-shielded 44-conductor I/O cable.

ATA standards require 80-conductor cables to be used for Ultra DMA modes 3 through 5. The length of the cable shall not exceed 18 inches.

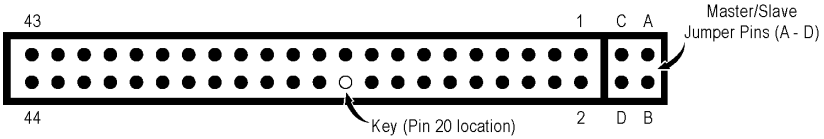

Figure 2. *44-pin ATA (IDE) Bus Connector*

2.1.1.2 IDE Interface Connector Pinout Configuration

Table 3 on page 12 provides the signal assignments for the 44-pin ATA bus connector (Figure 2 on page 11).

Table 3. *ATA (IDE) Connector Pinout Configuration*

Pin	Pin Type	Signal Symbol	Signal Name	Signal Description
1	I	-RESET	HOST RESET	Reset signal from the host. Reset is active on power up and inactive thereafter.
2	Ground	GND	—	Ground
3	I/O	D07	HOST DATA 7	Pins 3 through 18 (16 lines (15-0)) carry the data between the controller and the host. The low 8 lines transfer commands and the ECC information between the host and the controller.
4	I/O	D08	HOST DATA 8	
5	I/O	D06	HOST DATA 6	
6	I/O	D09	HOST DATA 9	
7	I/O	D05	HOST DATA 5	
8	I/O	D10	HOST DATA 10	
9	I/O	D04	HOST DATA 4	
10	I/O	D11	HOST DATA 11	
11	I/O	D03	HOST DATA 03	
12	I/O	D12	HOST DATA 12	
13	I/O	D02	HOST DATA 02	
14	I/O	D13	HOST DATA 13	
15	I/O	D01	HOST DATA 01	
16	I/O	D14	HOST DATA 14	
17	I/O	D00	HOST DATA 0	
18	I/O	D15	HOST DATA 15	
19	Ground	GND	—	Ground
20	—	—	—	No connection. Reserved for connector key.
21	O	DREQ	DMA REQUEST	Not used
22	Ground	GND	—	Ground
23	I	-IOWR	I/O WRITE	This I/O Write strobe pulse is used to clock I/O data or commands on the drive data bus into the Drive controller registers when the drive is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
24	Ground	GND	—	Ground

Continued

Table 3. *ATA (IDE) Connector Pinout Configuration (Continued)*

Pin	Pin Type	Signal Symbol	Signal Name	Signal Description
25	I	-IORD	I/O READ	This is a Read strobe generated by the host. The signal gates I/O data or status on the host bus and strobes the data from the controller into the host on the low to high transition (trailing edge).
26	Ground	GND	—	Ground
27	I	IORDY	I/O READY	Not used, and pulled up to Vcc through a 4.7k ohm resistor.
28	I	-CSEL	CABLE SELECT	This internally pulled up signal is used to configure the drives as the Master or the Slave device. When the pin is grounded, the device is configured as a Master. When the pin is open, the device is configured as a Slave.
29	I	-DACK	DMA ACKNOWLEDGE	Not used
30	Ground	GND	—	Ground
31	O	INTRQ	INTERRUPT REQUEST	This is an interrupt request from the controller to the host, asking for service. This signal is the active high Interrupt Request to the host.
32	O	-IOS16	I/O SELECT 16	Not used
33	I	A1	HOST ADDRESS 1	This address line (A1) is used to select one of eight registers in the controller Task File.
34	I/O	-PDIAG		After an Executive diagnostic command to indicate to the Master it has passed its diagnostics, this bi-directional open drain signal is asserted by the Slave.
35	I	A0	HOST ADDRESS 0	These address lines (A0 and A2) are used to select one of eight registers in the controller Task File.
36	I	A2	HOST ADDRESS 2	
37	I	-CS1	HOST CHIP SELECT 1	The chip select signal used to select the Task File register.
38	I	-CS2	HOST CHIP SELECT 2	The chip select signal used to select the Alternate Status register and the Device Control register.
39	I/O	-DASP	DISK ACTIVE/SLAVE PRESENT	This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
40	Ground	GND	—	Ground

Continued

Table 3. *ATA (IDE) Connector Pinout Configuration (Continued)*

Pin	Pin Type	Signal Symbol	Signal Name	Signal Description
41	—	V_{CC}	Supply Voltage	5V power supply
42	—	V_{CC}	Supply Voltage	5V power supply
43	Ground	GND	—	Ground
44	—	—	—	No connection

2.1.2 SSD Control Block

The Panther PATA SSD's control block comprises four integrated components:

- Memtech Panther SSD controller
- RISC Microcontroller
- Channel Controller
- NAND SLC flash memory

Memtech's Panther FPGA (Field Programmable Gate Array) controller is the heart of the Panther PATA SSD. The Panther controller provides the drive's ATA interface to the host, and the IDE interface to the drive's local flash memory. The Panther controller's integrated DMA controller interfaces with system memory to facilitate data transfer between the host and the SSD's local flash memory.

An integrated microcontroller is responsible for initiating and controlling all activity within the Panther ATA controller. The microcontroller features more than 2 Mbits of on-chip SRAM supporting a wide range of peripheral functions, with 16 Mbits of flash memory into a single compact 120-ball BGA package, providing a powerful and flexible solution for the SSD's embedded control applications. The SSD's embedded microcontroller is a high-performance processor with a high-density instruction set and very low power consumption. In addition, a large number of internally banked registers provide very fast exception handling—making it ideal for the real-time application control requirements of the SSD. The 8-level priority-vectored interrupt controller, together with the Peripheral Data Controller, significantly enhance the SSD's real-time performance.

The SSD's flash memory controller architecture requires only minimal external component support. The SSD's flash controller works with flash memory devices from Samsung® and Toshiba®, as well as a number of compatible flash memory devices from other manufacturers.

Features of the SSD's flash memory controller include:

- Built-in 3.3V voltage regulator for flash memory supply
- Data transfer rates up to 40 MB/sec (controller to flash memory)
- True-IDE mode support
- Embedded ECC unit
- Wear-leveling and bad-block mapping software

2.1.3 Flash Memory

The Panther PATA SSD's local storage subsystem uses Single-Level Cell (SLC) NAND, non-volatile flash memory. Having only two states and one bit of data stored, SLC NAND flash control logic on the SSD is able to conserve energy when managing the electrical charge during operations.

2.1.3.1 Storage Capacity

Table 4, provides a representative list of the various capacities in which Memtech's Panther PATA SSDs are available, along with associated LBA (Logical Bit Addressing) and CHS (Cylinder, Head, Sector) information.

Table 4. *Panther PATA SSD Capacity*

	Logical Bit Addressing (LBA) Data	Cylinder, Head, Sector (CHS) Data			
Capacity (GB) (unformatted)	**User-Addressable LBA Sectors**	**CHS Capacity**[a]	**Logical Cylinders**	**Logical Heads**	**Logical Sectors**
4 (4096 MB)	8022016	8021664	7958	16	63
8 (8192 MB)	16074752	16074576	15947	16	63
16 (16384 MB)	32180224	16514064	16383	16	63
24 (24576 MB)	48285696	16514064	16383	16	63
32 (32768 MB)	64393216	16514064	16383	16	63
64 (65536 MB)	128817152	16514064	16383	16	63

a. Expressed as LBA sectors

2.2 PRINCIPLES OF OPERATION

The Panther PATA SSD comprises four primary functional blocks—the ATA (IDE) interface and connector, Panther SSD controller, channel controller, and NAND flash memory. A description of each drive component is provided in “Panther PATA SSD Functional Blocks” on page 11.

All read/write data transfer requests are initiated by the host via the ATA (IDE) bus interface. Once received, the Panther controller, under the control of the SSD’s microcontroller, processes the request.

The SSD’s microcontroller is responsible for initiating and controlling all activity within the Panther controller—including bad block mapping and executing the wear-leveling algorithms.

The Panther controller decodes an incoming host command, and sets up the appropriate interrupts and status for the local microprocessor to handle various ATA commands. For read and write transfer commands, the hardware can handle the initial handshake with the host automatically. If firmware enables full auto mode, read and write transfers can be fully handled by hardware with minimum firmware support.

Commands that do not require data to be read from or written to the flash memory controller are typically handled by the Panther controller. Some commands may require the Panther controller to use external circuitry (for example, Intelligent Destructive Purge™), which do not involve the flash memory controller.

When a write operation is requested and data is received, the Panther controller uses integrated DMA controllers to transfer the data from host memory to the SSD’s flash memory controller. Through a standard ATA (IDE) interface, the flash memory controller transfers the data from the Panther controller to available locations in the SSD’s local flash memory. Depending on drive configuration, Panther PATA SSD storage capacity can range between from 4GB to 64GB, with internal IDE transfer rates ranging from 10 to 40 MB per second. After the write operation completes, the Panther controller notifies the host.

If a read request is received, the Panther controller retrieves the data from the local flash memory via the flash memory controller. If the Panther controller is responding to a PIO read operation, it presents the data to the ATA bus. If it is responding to a UDMA read request, the Panther controller writes the data directly to system memory on the host. Regardless of the type of operation (PIO or UDMA), the Panther controller notifies the host when the data is ready for transmission and when the transfer is complete.

2.3 OPERATING MODES

The Panther PATA SSD is configured as a high-performance I/O device, supporting the following operating modes:

- Primary drive address at system ATA I/O address 1F0h - 1F7h and 3F6h - 3F7h. The host must provide chip-enable #CS0 and #CS1. The SSD decodes addresses DA0 - DA2.
- Secondary drive address at system ATA I/O address 170h - 177h and 376h - 377h. The host must provide chip-enable #CS0 and #CS1. The SSD decodes addresses DA0 - DA2 to access individual Task File Registers.

2.3.1 I/O Primary and Secondary ATA (IDE) Modes

Primary and secondary drive addressing modes allow hosts to use the ATA-standard's reserved disk drive I/O addresses. This provides computer system designers with the simplest way to accommodate ATA-protocol devices.

2.3.1.1 Addressing Modes

Panther PATA SSDs, on a command by command basis, can operate in either CHS or LBA addressing modes. Identify Drive Information (see "Identify Drive Information" on page 20) tells the host whether the drive supports LBA mode. The host selects LBA mode via the Drive/Head register. Sector Number, Cylinder Low, Cylinder High, and Drive/Head register bits HS3=0 contain the zero-based LBA. The drive's sectors are linearly mapped with: LBA = 0 => Cylinder 0, head 0, sector 1. Regardless of the translation mode, a sector LBA address does not change. LBA = (Cylinder * no of heads + Head) * (sectors/track) + (Sector - 1). Table 5 on page 18 lists the supported IDE addressing modes.

Table 5. *ATA (IDE) Bus Addressing Modes*

#CS0	#CS1	DA2	DA1	DA0	#IORD = "0"	#IOWR - "0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate status	Device Control
1	0	1	1	1	Device address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

2.4 ATA COMMANDS

This section provides information on the ATA commands supported on the Panther PATA SSD. The commands are issued to the ATA by loading the required registers in the command block with the supplied parameter, and then writing the command code to the register.

2.4.1 ATA Command Flow

1 Write the necessary parameters to the related Task File Registers and by writing the command in the Command register, the transaction is started.

2 Upon the receipt of the command, the device sets the BSY bit within 400 n/sec.

3 If a data transfer command (e.g., Read command, Write command) is requested, the DRQ bit in the Status register goes active, indicating that the transfer can begin.

2.4.2 Standard ATA Commands

Table 6 lists each command along with its respective command code and registers accessed by the command. For detailed descriptions of the ATA commands, refer to the ATA-5 specification.

Table 6. *Supported ATA Commands*

Command	Command Code (Hex)	Feature Register	Sector Count Register	Sector Number Register	Cylinder High/Low Register	Drive/Head Number Register
CHECK POWER MODE	98 or E5	No	Yes	No	No	Yes [a]
ERASE SECTOR	C0	No	Yes	Yes	Yes	Yes [b]
EXECUTE DRIVE DIAGNOSTIC	90	No	No	No	No	Yes [c]
FORMAT TRACK	50	No	Yes	No	Yes	Yes (b)
IDENTIFY DRIVE	EC	Yes	No	No	No	Yes (a)
IDLE	97, E3	No	Y	No	No	Yes (a)
IDLE IMMEDIATE	95, E1	No	No	No	No	Yes (a)
INITIALIZE DRIVE PARAMETERS	91	No	Yes	No	No	Yes (b)
READ MULTIPLE	C4	No	Yes	Yes	Yes	Yes (b)
READ SECTOR(S)	20	No	Yes	Yes	Yes	Yes (b)
READ VERIFY SECTOR(S)	40	No	Yes	Yes	Yes	Yes (b)
RECALIBRATE	10	No	No	No	No	Yes (a)
SEEK	70 - 7F	No	No	Yes	Yes	Yes (b)
SET FEATURES	EF	No	Yes	Yes	Yes	Yes (b)
SET MULTIPLE MODE	C6	No	Yes	No	No	Yes (a)
SET SLEEP MODE	99 or E6	No	No	No	No	Yes (a)
STANDBY	96 or E2	No	Yes	No	No	Yes (a)
STANDBY IMMEDIATE	94 or E0	No	No	No	No	Yes (a)
WRITE MULTIPLE	C5	No	Yes	Yes	Yes	Yes (b)
WRITE SECTOR(S)	30	No	Yes	Yes	Yes	Yes (b)

a. Only drive parameters are valid.
b. Drive and head parameters are valid.
c. Address to drive 0 (zero). When executed, Both drives (master and slave) execute this command).

2.4.3 Optional ATA Command Support

2.4.3.1 SMART (Self-Monitoring, Analysis and Reporting Technology)

Panther PATA SSDs are designed to operate in mission-critical systems where remote monitoring of the drives's internal status is required, but removal of the drive for status checking is unacceptable. To provide remote monitoring support, Panther PATA SSDs can be programmed with the optional SMART feature. SMART enables the SSD to perform internal system monitoring, and report on the status of the drive. SMART is also used to analyze the SSD's bad-block status. The total number of bad blocks accumulated from the date of manufacture; relative to the disk total capacity, is returned as status information. Monitoring accumulated bad blocks over time provides an indication of drive reliability and the expected life span of the drive in the system in which it is installed.

2.4.3.2 Identify Drive Information

The Identify Drive command is used by the host to determine parameter information passed from the SSD. When the Identify Drive command executes, the SSD sets the BSY bit, prepares to transfer the 256 words of SSD identification data to the host, sets the DRQ bit, clears the BSY bit, and then generates an interrupt. The host can then transfer the data by reading the Data register. All reserved bits or words are all zero. Table 7 contains typical Identify Drive Information for the Panther PATA SSD.

Table 7. *SSD Identify Drive Information*

Word	Data	Total Bytes	Description
0	8040h	2	General configuration bit-significant information (value fixed by CFA)
1	XXXXh[a]	2	Default number of cylinders
2	0000h	2	Reserved
3	XXXXh (a)	2	Default number of heads
4	XXXXh (a)	2	Number of unformatted bytes per track (not used)
5	XXXXh (a)	2	Number of unformatted bytes per sector (not used)
6	XXXXh (a)	2	Default number of sectors per track
7-8	XXXXh(a)	4	Number of sectors per drive (Word7 = MSW, Word8 = LSW)
9	0000h	2	Reserved
10-19	XXXXh (a)	20	Serial number

continued

Table 7. *SSD Identify Drive Information (Continued)*

Word	Data	Total Bytes	Description
20	XXXXh [a]	2	Buffer type (dual ported, multi-sector, with read cache)
21	XXXXh [a]	2	Buffer size (in 512 byte increments)
22	XXXXh [a]	2	Number of ECC bytes passed on Read/Write Long Sector commands
23-46	XXXXh [a]	48	Firmware version and model number in ASCII
47	8001h	2	Maximum sector count = 1 on Read/Write Multiple commands
48	0000h	2	Double word not supported
49	2F00h	2	Capabilities: DMA not supported (bit 8); LBA supported (bit 9)
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0200h	2	Single word DMA data transfer cycle timing mode (not supported)
53	0007h	2	Words 54 - 58 and 64 - 70 are valid
54	XXXXh [a]	2	Number of current cylinders
55	XXXXh [a]	2	Number of current heads
56	XXXXh [a]	2	Number of current sectors per track
57	XXXXh [a]	2	LSW of the current capacity in sectors
58	XXXXh [a]	2	MSW of the current capacity in sectors
59	0000h	2	Current setting for block count = 1 for Read/Write Multiple commands
60-61	XXXXh [a]	4	Total number of user addressable sectors in LBA Mode
62	0000h	2	Single word DMA data transfer cycle timing mode not supported
63	0000h	2	Multi-word DMA modes active; modes 0 - 2 supported
64	0003h	2	Advanced PIO modes supported (modes 3 and 4)
65	0078h	2	Minimum multi-word DMA transfer cycle time per word (ns)
66	0078h	2	Recommended multi-word DMA transfer cycle time per word (ns)
67	00F0h	2	Minimum PIO transfer without flow control
68	0078h	2	Minimum PIO transfer with IORDY flow control
69-255	0000h	388	Reserved

a. Value varies depending on drive storage capacity.

2.4.4 Vendor-Specific ATA Commands

As with standard ATA commands, the software requirements and syntax of the vendor-specific ATA commands the host issues to the Panther PATA SSD are issued by loading the required registers in the command block with the required parameters, and then writing the command code to the register.

For additional information on proprietary Memtech ATA commands, contact your Memtech representative. Contact information is provided in “Contact and Ordering Information” on page 28.

2.4.4.1 Sanitize Erase/Fill

Panther PATA SSDs offer optional destructive and non-destructive sanitization (purge) features. Non-destructive security erase removes the drive’s data, then overwrites (fills) each addressable block of memory with a predetermined pattern, as specified by the sanitization specification, such as DoD 5220.22M, to which the SSD complies.The destructive security erase feature removes the drive’s data, and then destroys the flash media—making the SSD totally unusable and data retrieval impossible. Memtech’s non-destructive and patent-pending destructive security erase algorithms monitor and confirm completion of the sanitization process.

Both security erase features support Low Power and Fast Erase options. The Low Power option accesses each addressable memory block sequentially to conserve power. The Fast Erase option accesses all addressable blocks simultaneously, forgoing power conservation for speed.

2.4.4.2 Sanitization Standards

Panther PATA SSDs comply with the sanitization requirements described in Table 8.

Table 8. *Sanitize Standards Compliance*

Specification	Document Description/Comment
USA DoD 5220.22-M National Industrial Security Program Operation Manual (NISOM) January 1995	Specifies the sanitization process for various media types in order to be considered declassified.
NSA 130-2 Media Declassification and Destruction Manual November 2000	Specifies the sanitization procedure for semiconductor memory devices.
AR 380-19 Information Systems Security (ISS) 27 March 1998	Provides the security requirements for systems processing Special Access Program (SAP) information and describes the ISS policy as it applies to security in hardware, software procedures, telecommunication, personal use, physical environment, networks and firmware. Section VII, Automated Information System Media, Section 2-20, describes cleaning, purging, declassifying and destroying media. Appendix F-2 describes how to sanitize flash memory.
AFSSI 5020 USA Air Force System Security Instruction (AFSSI) 5020 20 August 1996	Specifies the sanitization procedure for confidential media. Chapter 5, Semiconductor Devices, describes the security procedure for all types of semiconductor media. Paragraph 5.3 describes the procedure for sanitizing flash memory.
Navso P-5239-26 Information Systems Security (INFOSEC) Program Guidelines	Provides policy, guidelines, and procedures for clearing and purging computer system memory and other storage media for release outside of and for reuse within controlled environments. It pertains to both classified and sensitive unclassified information. Implements DOD 5200.28-M and CSC-STD-005-85. Chapter 3 describes the cleaning and purging of data storage media.

3 INSTALLATION

3.1 SYSTEM REQUIREMENTS

Before installing the Panther PATA SSD in your system, make sure you have the following items:

- Mounting hardware (as required)
- ATA (IDE) bus interface cable (as specified in Table 9, below)

Table 9. *ATA (IDE) Cable Requirements*

ATA (IDE) Interface	Operating Mode
44-pin; 44 conductor	PIO modes 0, 1, 2, 3 and 4 Ultra DMA modes 0, 1 and 2
44-pin 80-conductor	Ultra DMA modes 3 and 4

3.2 DRIVE CONFIGURATION

Before installing the SSD, the drive must be configured to operate as either the Master or Slave IDE device. The Master/Slave setting represents the ordering of electronic devices on an IDE channel. If the Panther PATA SSD is the only ATA (IDE) drive installed in the system, set up the drive as the master device. If two drives are installed in the machine, one device must be configured as the master and the other as the slave. Jumpers located at the rear of the Panther PATA SSD allow you to configure the drive as either the Master or the Slave device.

3.2.1 Configuring 2.5-inch Form Factor Panther PATA SSD

The 2.5-inch Panther PATA SSD is equipped with a 44-pin ATA bus connector. To configure the SSD as either the Master or Slave device, place a jumper across the appropriate pins (A - D) as illustrated in Figure 3 on page 26.

In systems with multiple drives, it may be necessary to configure disk storage in a Master/Slave configuration. To accomplish this, boot the computer using IDE HDD Auto Detection available in the CMOS setup.

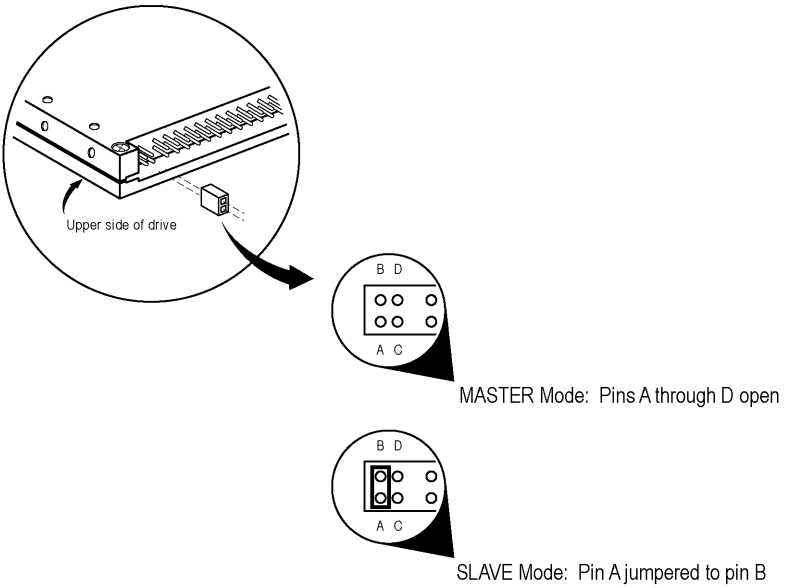

Figure 3. *Master/Slave Setting for 2.5-inch Panther PATA SSDs*

3.3 INSTALLING PANTHER PATA SSDS

To install the Panther PATA SSD in a personal computer (PC) or host system, complete the following steps:

1 Power down the computer and remove the access cover.

2 Configure the Panther PATA SSD as the master or slave device in accordance with the information provided in “Drive Configuration” on page 25.

3 Connect one end of an ATA (IDE) cable to the Panther PATA SSD and the other end of the cable to the IDE adapter on the host. Orient the cable so that pin 1 on the Panther SSD connects to pin 1 on the host adapter.

ATA standards require 80-conductor cables to be used for Ultra DMA modes 3 through 5. The length of the cable shall not exceed 18 inches (0.4572 meters).

For optimal performance, the recommended maximum length should not exceed 12 inches (0.3048 meters).

4 Position the Panther PATA SSD in an unused drive bay and secure it in place using six (6) machine screws. Apply sufficient torque to ensure that the drive is secure.

5 Replace the access cover and power on the computer.

3.3.1 Formatting Panther PATA SSDs for Windows, Linux and Other OS Environments

After installing the Panther PATA SSD (see section “Installing Panther PATA SSDs” on page 27), it is ready for use. Panther PATA SSDs do not require special driver installation, adjustments or modifications.

Panther SSDs are low-level formatted at the factory. However, the SSD must be partitioned and high-level formatted in the system in which it will be used.

3.4 UPGRADING PANTHER PATA SSD FIRMWARE

The firmware on the Panther PATA SSD is field upgradeable. Please contact Memtech for additional information and support.

CONTACT AND ORDERING INFORMATION

CONTACTING MEMTECH

For more information on Panther PATA SSDs, contact Memtech SSD Corp.

Phone: 800-445-5511 (Toll free; US and Canada only); (925) 294-8483
Fax: (925) 294-5920
Email: info@memtech.com

ORDERING INFORMATION

How to read Panther SSD part numbers:

XX YYYY G -ZZZZZ OPT

XX - Product Code

AT - Parallel ATA

SA - Serial ATA

YYYY - Series/Form Factor

258X - 2.5-inch form factor, Panther

358X - 3.5-inch form factor, Panther

G - Temperature Grade

Blank - Commercial (0° to 70° C)

I - Industrial (-40° to +85° C)

-ZZZZZZ - Raw Capacity in Megabytes (64 MB to 60000 MB)

OPT - Options

C - Conformal coat

NN - Custom

Example part number: (XX YYYY G ZZZZZ O)

AT2582I-4096C

- 2.5” PATA, IDE Panther
- Industrial (-40° to +85° C) temperature rating
- 4096 Mbytes
- Conformal coat

ACRONYMS AND ABBREVIATIONS

A

ARM (Advanced RISC Machine) <processor> (ARM, Originally Acorn RISC Machine). A series of low-cost, power-efficient 32-bit RISC microprocessors for embedded control, computing, digital signal processing, games, consumer multimedia and portable applications.

ATA (AT Attachment) The IDE interface is officially known as the ATA specification. ATA-2 (Fast ATA) defined the faster transfer rates used in Enhanced IDE (EIDE). ATA-3 added interface improvements, including the ability to report potential problems (see S.M.A.R.T.). Starting with ATA-4, either the word "Ultra" or the transfer rate was added to the name in various combinations. For example, at 33 MBytes/ sec, terms such as Ultra ATA and ATA-33 have been used. In addition, Ultra ATA-33, DMA-33 and Ultra DMA-33 are also found.

C

CFA (Computer Fraud and Abuse Act of 1986) The CFA was a significant step forward in criminalizing unauthorized access to computer systems and networks. The Act applies to "federal interest computers" which include systems used by the U.S. government, as well as most financial institutions. The Act makes unauthorized penetration or other damage to such systems a felony.

CHS Cylinder, Head, Sector A disc-drive system and method for generating logical zones that each have an approximate number of spare sectors, and that are used to translate logical block addresses.

CISC (Complex Instruction Set Computer) Pronounced "sisk." The traditional architecture of a computer which uses microcode to execute very comprehensive instructions. Instructions may be variable in length and use all addressing modes, requiring complex circuitry to decode them.

D

DMA (Direct Memory Access) Specialized circuitry or a dedicated microprocessor that transfers data from memory to memory without using the CPU. Although DMA may periodically steal cycles from the CPU, data are transferred much faster than using the CPU for every byte of transfer.

DoD (Department of Defense) The military branch of the U.S. government, which is under the direction of the Secretary of Defense, the primary defense policy adviser to the President.

DSL (Digital Subscriber Line) A technology that dramatically increases the digital capacity of ordinary telephone lines (the local loops) into the home or office. DSL speeds are tied to the distance between the customer and the telco central office (CO). DSL is geared to two types of usage. Asymmetric DSL (ADSL) is for Internet access, where fast downstream is required, but slow upstream is acceptable. Symmetric DSL (SDSL, HDSL, etc.) is designed for short haul connections that require high speed in both directions.

DSLAM (DSL Access Multiplexer) A central office (CO) device for ADSL service that combines voice traffic and DSL traffic onto a customer's DSL line. It also separates incoming phone and data signals and directs them onto the appropriate carriers network.

E

EDC/ECC (Error Detection Code/Error Correction Code) A memory system that tests for and corrects errors automatically, very often without the operating system being aware of it. When writing the data into memory, ECC circuitry generates checksums from the binary sequences in the bytes and stores them in an additional seven bits of memory for 32-bit data paths or eight bits for 64-bit paths. When data are retrieved from memory, the checksum is recomputed to determine if any data bits have been corrupted. Such systems can typically detect and automatically correct errors of one bit per word and can detect, but not correct, errors greater than one bit.

F

FPGA (Field Programmable Gate Array) A type of gate array that is programmed in the field rather than in a semiconductor fabrication facility. Containing up to hundreds of thousands of gates, there are a variety of FPGA architectures on the market. Some are very sophisticated, including not only programmable logic blocks, but programmable interconnects and switches between the blocks. The interconnects take up a lot of FPGA real estate, resulting in a chip with very low gate density compared to other technologies.

H

HDD (Hard Disk Drive) The primary computer storage medium, made of one or more aluminum or glass platters, coated with a ferromagnetic material. Most hard disks are "fixed disks," which have platters that reside permanently in the drive.

I

I/O (Input/Output) Transferring data between the CPU and a peripheral device. Every transfer is an output from one device and an input into another.

IDE (Integrated Drive Electronics) A type of hardware interface widely used to connect hard disks, CD-ROMs and tape drives to a PC. IDE was always the more economical interface, compared to SCSI. Starting out with 40MB capacities years ago, 20GB IDE hard disks have become entry level, costing a fraction of a cent per megabyte.

IO (Input/Output; see I/O)

L

LBA (Logical Block Addressing) A method used to support IDE hard disks larger than 504MB (528,482,304 bytes) on PCs. LBA provides the necessary address conversion in the BIOS to support drives up to 8GB. BIOS after mid-1994, which are sometimes called "Enhanced BIOS," generally provide LBA conversion. LBA support is required for compatibility with the FAT32 directory.

LSB (Least Significant Byte) "Byte" defines a sequence of 8-bits, with the right-most bit being the least significant and the left-most bit being the most-significant.

LSW (Least Significant Word) "Word" denotes sequence of 4 bytes, or 32 bits, with the left-most being the least significant, and the right-most being the most significant. "Double-word" denotes sequence of two words, or 64bits, with the left most word being the least significant, and the right-most - the most significant. Note, that the definition of "word" defines a little-endian scheme, so for big-endian platforms, or network applications, special steps need to be taken to reorder the bytes form the input stream.

M

MLC (Multi-Level Cell) A flash memory technology that stores more than one bit of data per cell. Traditional flash memory defines a 0 or 1 bit, based on a single voltage threshold. The patterns of two bits (0-0, 0-1, 1-0, and 1-1) can be achieved with four voltage levels and eight levels of voltage can yield all the combinations in three bits.

MSB (Most Significant) "byte" defines a sequence of 8-bits, with the right-most bit being the least significant and the left-most bit being the most-significant.

MSW (Most Significant Word) "Word" denotes sequence of 4 bytes, or 32 bits, with the left-most being the least significant, and the right-most being the most significant. "Double-word" denotes sequence of two words, or 64bits, with the left most word being the least significant, and the right-most - the most significant. Note, that the definition of "word" defines a little-endian scheme, so for big-endian platforms, or network applications, special steps need to be taken to reorder the bytes form the input stream.

N

NAND (Not AND) A Boolean logic operation that is true if any single input is false. Two-input NAND gates are often used as the sole logic element on gate array chips, because all Boolean operations can be created from NAND gates.

P

PIO (Programmed Input/Output) The data transfer mode used by IDE drives. PIO modes use the CPU's registers for data transfer in contrast with DMA, which transfers directly between main memory and the peripheral device.

R

RISC (Reduced Instruction Set Computer) A computer architecture that reduces chip complexity by using simpler instructions. RISC compilers have to generate software routines to perform complex instructions that were previously done in hardware by CISC computers. In RISC, the microcode layer and associated overhead is eliminated.

S

SLC Single-Level Cell A flash memory technology that stores one bit of data per memory cell; supporting only two states: erased (1) or programmed (0).

SMART (Self-Monitoring Analysis and Reporting Technology) An "early warning system" for anticipating pending drive problems. The drive's integrated controller works with various sensors to monitor several aspects of the drive's performance. Using this status information, SMART determines if the drive is behaving normally or not, and then makes the information available to software that probes the drive.

SSD (Solid State Disk) Disk drive that uses memory chips instead of rotating platters for data storage. Used in battery-powered handheld devices as well as desktop computers and servers, solid state disks (SSDs) are faster than regular disks because there is zero latency (there is no read/write head to move). They are also more rugged than hard disks and offer greater protection in hostile environments.

T

True-IDE Flash memory devices (such as CF cards) have a pin that when connected to the proper voltage at power-up selects the "True-IDE" mode of operation instead of the "PC-CARD-ATA" mode of operation. This is the mode used in the interface.

U

Ultra ATA An enhanced version of the IDE interface that transfers data at 33, 66 or 100 Mbytes/sec. These enhancements are also called "Ultra DMA," "UDMA," "ATA-33," "ATA-66," "ATA-100," "DMA-33," "DMA-66" and "DMA-100."

Ultra DMA (see Ultra ATA)

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WARRANTY

Limited Lifetime Warranty

Memtech warrants your Panther PATA SSD against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair.

The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered.

In no event shall Memtech be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM MEMTECH.

Product shall be returned to Memtech with shipping prepaid. If the product fails to conform and warranty repair is necessary, Memtech will reimburse customer for the transportation charges incurred.

Modifications

Any changes or modifications made to this device that are not expressly approved by Memtech, void the user's warranty. All wiring external to the product should follow the provisions of the current edition of the National Electrical Code.

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